

In the Specification

The following is a marked-up version of the specification with the language that is underlined (“ ”) being added and the language that contains strikethrough (“~~—~~”) being deleted:

For the paragraph beginning at page 4, line 15:

~~In one example application, the frequency divider of the invention is a component of a frequency synthesizer which in turn is a component of a transceiver. The transceiver, in turn, may be a component of a wireless communications device, including a mobile wireless communication device such as a mobile wireless handset. The device in turn may be included in a wireless communications system of the type in which a geographical area is divided into a plurality of cells, and a base station is included within each cell. The base station for a cell communicates with one or more mobile wireless devices within the cell through a wireless communications interface.~~

For the paragraph beginning at page 4, line 24:

~~In another example application, the frequency divider of the invention is a component of a translation loop which forms the transmitter section of a transceiver. The transceiver, in turn, may be a component of a wireless communications device, including a mobile wireless communication device such as a mobile wireless handset. The device in turn may be included in a wireless communications system of the type in which a geographical area is divided into a plurality of cells, and a base station is included within each cell. The base station for a cell communicates with one or more mobile wireless devices within the cell through a wireless communications interface.~~

For the paragraph beginning at page 5, line 4:

~~A related method of operation for a storage element in accordance with the subject invention comprises the steps of triggering upon a first edge of the clock signal if the desired division ration N has a first predetermined characteristic or the data output of the storage element is in a first predetermined state, and triggering upon a second edge of the clock signal if the desired division ration N has a second predetermined characteristic and the data output of the storage element is in a second predetermined state. In one implementation, the first predetermined characteristic of the division ratio is that it be an even integer, and the second predetermined characteristic of the division ratio is that it be an odd integer. In addition, in this implementation, the first predetermined state of the data output of the storage element is a logical low, and the second predetermined state of the data output of the storage element is a logical high. In one example, the first edge of the clock signal is a rising edge, and the second edge of the clock signal is a falling edge.~~

For the paragraph beginning at page 10, line 18:

Each of the flip-flops, 1, 2, 3, 4 also provides an output signal $/Q$ which is in the inverse of the data output signal Q . Each of these output signal $/Q$ is provided as a data input to multiplexor 49 2 through signal lines 18a, 18b, 18c, 18d. Collectively, these inputs are identified with numeral 12. Control inputs P_0 and P_1 , identified with numeral 13, are also provided as inputs to multiplexor 49 2. The output of multiplexor 49 2 is coupled to the data input of flip-flop 1, the first flip-flop in the sequence, through signal line 14. Multiplexor 49 2 switches one of the data inputs 12 to signal line 14, and thus to the data input of flip-flop 1, responsive to the state of the control inputs 13.

For the paragraph beginning at page 10, line 27:

Through suitable setting of the control inputs 13, the number of storage elements F which contributes to the frequency division function can be less than the number of storage elements which are physically present in the sequence. In one implementation, the number F of storage elements required to achieve a given division ration N is calculated using the formula presented earlier:

$$F = \frac{N + P}{2}$$

where P is 1 if the division ratio is odd, and 0 if the division ratio is even. Then, a series of F elements in the physical sequence is selected, and the inverse /Q of the data output of the Fth storage element in the series is coupled to the data input of the first storage element in the series through suitable settings of the control inputs 13 to multiplexor ~~49~~ 9.

For the paragraph beginning at page 28, line 4:

Figure 7 illustrates an implementation example of module 404 in Figure 6. As illustrated, the BIAS signal, identified with numeral 309, is coupled to the collector of transistor 502, which in turn coupled to its base. The emitter of transistor 502 is coupled to ground through resistor 503. Similarly, the BIAS signal is also coupled to the bases of transistors 506, 512, and ~~524~~ 514, the emitters of which are coupled to ground through resistors 507, 513, and 515 respectively.

For the paragraph beginning at page 29, line 31:

The BIASCM signal is coupled to the base of transistor 600, which is also coupled to its collector. The emitter of transistor 600 is couple to the collector of transistor 618 which is also

coupled to its base. The emitter of transistor 618 is coupled to ground through resistor 617. The collector of transistor 600 is also coupled to one end of resistor 601, and to one end of resistor ~~601~~ 602.

For the paragraph beginning at page 33, line 10:

A method of operation of a frequency divider in accordance with the subject invention is illustrated in Figure 12C. In step ~~800~~ 900, the required number of stages F are placed in a ring, such that the input to a given stage is an output from a previous stage, and the input to the first stage is an output from the last stage.

For the paragraph beginning at page 33, line 14:

In step ~~801~~ 901, a determination is made whether there is a transition of the input to one of the stages. If not, a loop is made to the beginning of step ~~801~~ 901. If so, step ~~802~~ 902 is performed.

For the paragraph beginning at page 33, line 17:

In step ~~802~~ 902, if the given stage is other than a selected stage in the ring, the given stage produces a transition on its output signal which lags that of its input signal by one full clock cycle and which is in the same direction, either low-to-high or high-to-low, as that transition. In one embodiment, the selected stage is in the first stage. Step ~~803~~ 903 is then jumped to.

For the paragraph beginning at page 33, line 22:

In step ~~803~~ 903, if the given stage is the selected stage in the ring, the given stage produces a transition on its output signal which lags that of its input signal by one-half a clock cycle and which is in the opposite direction as that transition.

For the paragraph beginning at page 33, line 25:

A jump is then made to the beginning of step ~~804~~ 901, wherein the process repeats itself at that point.